CLAIMS

1. An active matrix display, comprising:

an array (34) of pixels provided over a common substrate (44), each pixel comprising a display element (16) and a switching device (14), and the array of pixels defining a display area (63) and the pixels being formed from a plurality of thin film layers (10,11,78,74,80);

column driver circuitry (32) for providing signals to the pixels for driving the display elements; and

row driver circuitry (30) for providing signals to the pixels for controlling the switching devices of the pixels,

wherein the display further comprises at least one conductor line (62a,62b,62c) extending along an edge of the display over the common substrate (44) and outside the display area (63), the at least one conductor line comprising at least one layer (90) additional to the plurality of thin film layers defining the array of pixels, and wherein at least one of the row driver circuitry (30) and the column driver circuitry (32) comprises a portion (40,50) provided on the common substrate (44) outside the display area (63) and which connects to the at least one conductor line (62a,62b,62c).

2. A display as claimed in claim 1, wherein the portion (40,50) of the at least one of the row driver circuitry and the column driver circuitry comprises an integrated circuit provided on the common substrate outside the display area.

3. A display as claimed in claim 2, wherein the row driver circuitry (30) comprises at least one row driver integrated circuit (40) mounted on the common substrate (44), and wherein the at least one conductor line (62a,62b) is parallel to a side edge of the display.

4. A display as claimed in claim 3, wherein the at least one conductor line comprises a plurality of lines (62a,62b) parallel to the side edge of the display.

5. A display as claimed in claim 2, wherein the column driver circuitry (32) comprises at least one column driver integrated circuit mounted (50) on the common substrate (44), and wherein the at least one conductor line (62c) is parallel to a top edge of the display.

6. A display as claimed in claim 5, wherein the at least one conductor line (62c) comprises a plurality of lines parallel to the top edge of the display.

7. A display as claimed in claim 5 or 6, wherein the column driver circuitry further comprises a column driver printed circuit board (58) which connects to the at least one column driver integrated circuit (50).

8. A display as claimed in any preceding claim, wherein the at least one conductor line (62a,62b,62c) comprises a plated line formed over a support (70) defined by one or more of the plurality of thin film layers.

9. A display as claimed in any one of claims 1 to 7, wherein the at least one conductor line (62a,62b,62c) comprises a printed line.

10. A display as claimed in any preceding claim, wherein the at least one conductor line (62a,62b,62c) comprises a power supply line.

11. A display as claimed in any preceding claim, wherein each pixel further comprises a storage capacitor (20) connected between the display element (16) and a common storage capacitor line (22), and the at least one conductor (62a,62b,62c) line comprises the storage capacitor line.

12. A display as claimed in any preceding claim, wherein the at least one conductor line (62a,62b,62c) comprises a clock signal line.

13. A method of fabricating an active matrix display, comprising:

forming an array of pixels over a common substrate (44) within a display area of the substrate, each pixel comprising a display element (16) and a switching device (14);

subsequently forming at least one conductor line (62a,62b,62c) extending along an edge of the display over the common substrate (44) and outside the display area (63); and

connecting row driver circuitry or column driver circuitry to the at least one conductor line.

14. A method as claimed in claim 13, wherein the row driver circuitry or the column driver circuitry comprises an integrated circuit (40,50), and connecting comprises mounting the integrated circuit on the substrate and providing electrical connections to the at least one conductor line.

15. A method as claimed in claim 13 or 14, wherein the at least one conductor line is formed by plating over one of layers forming the array of pixels.

16. A method as claimed in claim 15, wherein the plating is over a thin film metal layer (10) used to form row conductors in the pixel array.

17. A display as claimed in claims 13 or 14, wherein the at least one conductor line is formed by printing.